What is claimed is:

1. An integrated excitation/extraction system for test and measurement of a circuit under test (CUT) on a chip, the system comprising:

a signal generator integrated on the chip for generating a test signal for exciting the CUT; and

a signal digitizer integrated on the chip for extracting a digital signal for test and measurement from a response signal received from the CUT.

2. The system of claim 1 wherein the signal generator comprises a memory circuit for generating the test signal as a periodic ΣΔ bitstream test signal.

3. The system of claim 2 further comprising an analog reconstruction filter for receiving the periodic ΣΔ bitstream and generating a filtered test signal for communicating to the CUT.

4. The system of claim 3 wherein the reconstruction filter is integrated on the chip.

5. The system of claim 4 further including a means for communicating the filtered test signal to the signal digitizer while bypassing the CUT.

6. The system of claim 2 wherein the memory circuit comprises a sequential shift register.

7. The system of claim 1 wherein the signal generator comprises means for programming the test signal.

8. The system of claim 1 wherein the signal digitizer comprises:

a reference voltage generator for generating a variable DC reference voltage signal; and

a comparator for extracting the digital signal in response to the comparison of the response signal and the reference voltage.

9. The system of claim 8 wherein the signal digitizer further comprises a first means for sub-sampling the response signal for communicating to the comparator.

10. The system of claim 9 wherein the signal digitizer further comprises a second means for sub-sampling the reference voltage signal for communicating to the comparator.

11. The system of claim 8 wherein the reference voltage generator comprises:

a voltage signal generator for encoding a DC voltage level in a periodic bit-stream signal; and

an averaging circuit to extract the DC reference voltage from the periodic signal.

12. The system of claim 11 wherein the periodic bit-stream signal is a pulse density modulation signal.

13. The system of claim 11 wherein the voltage signal generator comprises a sequential shift register.

14. The system of claim 8 wherein the reference voltage generator comprises means for programming the reference voltage signal.

15. The system of claim 11 wherein the averaging circuit is a passive RC filter.

16. The system of claim 1 wherein the signal digitizer comprises memory means for storing the digital signal.

17. The system of claim 16 wherein the memory means is integrated on the chip.

18. The system of claim 16 wherein the memory means comprises a multi-bit memory having a length at least as long as the length of a unit test period for sampling the response signal.

19. The system of claim 1 further comprising a control means for synchronously controlling the signal digitizer and signal generator.

20. The system of claim 19 wherein the control means is integrated on the chip.

21. The system of claim 19 further comprising programming means for programming the system wherein the signal digitizer is programmed and controlled to extract the digital signal in response to a plurality of samples of the response signal.

22. The system of claim 1 wherein the signal generator comprises a first memory circuit for generating the test signal; wherein the signal digitizer comprises a second memory circuit for generating a DC reference voltage for digitizing the response signal and wherein the first and second memory circuits comprise a single scan-chain integrated on the chip.

23. The system of claim 22 wherein the signal digitizer further comprises a third memory circuit for storing the digital signal and wherein the first, second and third memory circuits comprise a single scan-chain integrated on the chip.

24. The system of claim 1 for test and measurement of a plurality of circuits under test and wherein the system comprises a plurality of signal generators and a

plurality of signal digitizers and wherein the system further comprises a means for programming said signal generators and signal digitizers whereby said system is operable to selectively test and measure said circuits under test.

25. The system of claim 1 further comprising a digital signal processor (DSP) for processing the digital signal.

26. An method for excitation/extraction for test and measurement of a circuit under test (CUT) on a chip, the method comprising the steps of:

generating a test signal for exciting the CUT by a signal generator integrated on the chip; and

extracting a digital signal for test and measurement from a response signal received from the CUT, by a signal digitizer integrated on the chip.

27. The method of claim 26 wherein the step of generating comprises a generating the test signal as a periodic ΣΔ bitstream.

28. The method of claim 27 wherein the step of generating further comprises filtering the periodic ΣΔ bitstream and generating a filtered test signal for communicating to the CUT.

29. The method of claim 28 wherein the steps of reconstruction filtering is performed on the chip.

30. The method of claim 29 further including the step of communicating the filtered test signal to the signal digitizer while bypassing the CUT.

31. The method of claim 26 further including the step of programming the signal generator with the test signal.

32. The method of claim 26 wherein the step of extracting comprises:

generating a variable DC reference voltage signal; and

comparing the response signal and the reference voltage to digitize the digital signal.

33. The method of claim 32 wherein the step of comparing further comprises sub-sampling the response signal.

34. The method of claim 33 wherein the step of comparing further comprises sub-sampling the reference voltage signal.

35. The method of claim 32 wherein the step of generating comprises:

generating a signal encoding a DC voltage level in a periodic bit-stream signal; and

averaging the periodic bit-stream signal to extract the DC reference voltage.

36. The method of claim 35 wherein the periodic bit-stream signal is a pulse density modulation signal.

37. The method of claim 32 further comprising the step of programming the reference voltage signal.

38. The method of claim 35 wherein the step of averaging comprises is a passively filtering the periodic bit-stream.